REMARKS/ARGUMENTS

Claims 1, 3-17, and 19-31 are pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of these remarks/arguments.

Claims 24 and 25 are allowed. In paragraph 3, the Examiner rejected claims 1, 3-5, 9, 13-14, 17, 19, 22-23, and 26-31 under 35 U.S.C. § 103(a) as being unpatentable over Givehchi in view of Nagata. In paragraph 4, the Examiner rejected claims 1, 3-5, 8-9, 13-14, 17, 19, 22-23, and 26-31 under 35 U.S.C. § 103(a) as being unpatentable over Walklin in view of Nagata. In paragraph 5, the Examiner objected to claims 6-7, 10-12, 15-16, and 20-21 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form. For the following reasons, the Applicant submits that all pending claims are allowable over the cited references.

Claim 1 is directed to an apparatus for converting a non-return-to-zero (NRZ) data signal to a return-to-zero (RZ) data signal. The apparatus comprises an amplifier configured to generate an amplified RZ data signal corresponding to the NRZ data signal based on (i) the NRZ data signal and (ii) a clock signal synchronized with the NRZ data signal. The amplifier is a differential amplifier configured to generate the amplified RZ data signal based on a comparison between a first signal corresponding to the NRZ data signal and a second signal corresponding to the clock signal, wherein there is a DC offset between the first and second signals.

Givehchi discloses an optical apparatus for generating an RZ optical data stream using an NRZ data signal. A representative embodiment of this apparatus is shown in Givehchi's Fig. 2. More specifically, the apparatus has Mach-Zehnder modulator **204** configured to receive drive signal **217** from driver **232**, where the drive signal is generated based on output signal **236** of generator **240.** Generator **240** includes AND-gate **241** configured to apply a logic AND function to the binary input data (first) and clock (second) signals, thereby generating signal **236.** In the rejection of claim 1, on page 2 of the office action, the Examiner admitted that "Givehchi does not specifically disclose there is a DC offset between the first and second signals." However, the Examiner then proceeded to state that "Nagata teaches a signal generator (2, fig. 1) that receives a NRZ signal (NRZ, fig. 1) and a clock signal (CK, fig. 1) to further generate a RZ signal (RZ, fig. 1), wherein a modulator (1, fig. 1) receives a multi-bit signal to which a DC offset value is added to output the NRZ signal."

Nagata discloses an over-sampling digital-to-analog converter (DAC) that can be configured to hold an average DC potential of its output signal at a predetermined value. A representative embodiment of this over-sampling DAC is shown in Nagata's Fig. 1, with a configuration employing a DC offset relied upon by the Examiner in the rejection of claim 1 being illustrated in Nagata's Fig. 7. Referring first to Nagata's Fig. 1, an RZ signal in the over-sampling DAC is generated by AND circuit **12**, which receives (i) the NRZ signal generated by ΣΔ modulator **1** and (ii) a clock (CK) signal received by the over-sampling DAC. Since AND circuit **12** compares the NRZ signal and the CK signal to generate the RZ signal, then, in the terminology of claim 1, the NRZ signal is the "first signal" and the CK signal is the "second signal." It therefore appears that, in the rejection of claim 1, the Examiner contends that there is a DC offset between the NRZ and CK signals applied to AND circuit **12**. For the following reasons, the Applicant submits that this contention is clearly wrong.

Nagata explicitly specifies voltage levels for the NRZ signal to be VDD and GND. More specifically, ΣΔ modulator **1** converts the received digital multi-bit signal into a digital binary ("one bit") NRZ signal (see Nagata's col. 6, lines 64-67). This NRZ signal has a high level equal to the

high power-supply level (labeled VDD) and a low level equal to the ground level (labeled GND, conventionally zero). See Nagata's Fig. 2, the second trace from the top, and col. 8, lines 6-9.

Nagata does not explicitly specify voltage levels for the CK signal (see, Nagata's Fig. 2). However, these voltage levels can be inferred from the functionality of AND circuit **12**, which processes the NRZ and CK signals to generate the RZ signal. More specifically, it is well known that an AND circuit is a logic circuit that converts two input voltages into one output voltage using the following conversion rules: LL→L, LH→L, HL→L, HH→H, where L is the logic low and H is the logic high. Since Nagata's Fig. 2 explicitly specifies that the RZ signal (the third trace from the top) generated by AND circuit **12** has voltage levels VDD and GND and we have already established above that the NRZ signal applied to the AND circuit by ΣΔ modulator **1** also has voltage levels VDD and GND, it follows from the above conversion rules that the CK signal similarly has voltage levels VDD and GND. Since we have now established that both the NRZ signal and the CK signal have voltage levels VDD and GND, it then follows that there is no DC offset between these signals, the Examiner's assertion to the contrary notwithstanding.

Referring now to Nagata's Fig. 7, the Applicant would like to emphasize the fact that, in the DAC configuration employing a DC offset, which was relied upon by the Examiner in the rejection of claim 1, the DC offset is added to the multi-bit input signal applied to ΣΔ modulator **1**, and <u>not</u> to the NRZ output signal applied to AND circuit **12** as it would be in an example of the apparatus recited in claim 1. Furthermore, the addition of this DC offset to the multi-bit input signal <u>does not alter</u> the NRZ output signal because ΣΔ modulator **1** is a differential circuit that cancels out any DC offsets by virtue of operating on signal differentials (see, e.g., elements Z^{-1} in Nagata's Fig. 13 that shows the circuit details of ΣΔ modulator **1**). As further explained by Nagata, adding a DC offset to the multi-bit input signal might be beneficial because such addition suppresses the overall circuit instability (parasitic beat generation) in an idling regime, i.e., when the multi-bit input signal has a relatively long sequence of uninterrupted zeros (see Nagata's Fig. 6 and col. 2, lines 30-48).

For all these reasons, the Applicant submits that the Examiner misinterpreted the teachings of Nagata and used them improperly to reject claim 1 and that claim 1 is allowable over Givehchi and Nagata. For similar reasons, the Applicant submits that claim 17 is also allowable over Givehchi and Nagata. Since claims 3-16, 19-23, and 26-31 depend variously from claims 1 and 17, it is further submitted that those claims are also allowable over Givehchi and Nagata.

Walklin discloses a return-to-zero (RZ) modulator for an optical transmitter. A representative embodiment of this optical transmitter is shown in Walklin's Fig. 3A. More specifically, Walklin's optical transmitter has Mach-Zehnder interferometer **2** that is controlled by a drive circuit having NRZ-to-RZ converter **30**. Converter **30** includes clocked trigger flip-flop **31** that receives NRZ (first) and clock (second) signals and is triggered "at roughly the middle of an NRZ data bit" to enable the NRZ-to-RZ signal conversion (Walklin's paragraph [0032]). Amplifier **32** is then used to boost the RZ signal produced by converter **30**, and optional low-pass filter **34** is used to adjust the rise and fall times of the pulses in the resulting amplified RZ signal.

In the rejection of claim 1, on page 5 of the office action, the Examiner admitted that "Walklin does not specifically disclose there is a DC offset between the first and second signals." The Examiner then attempted to remedy this admitted deficiency of Walklin by relying on the teachings of Nagata in substantially the same manner as in the preceding rejection of claim 1 over the combination of Givehchi and Nagata. In response the Applicant reiterates the above-explained reading of Nagata and submits that the Examiner misinterpreted the teachings of Nagata and used them improperly to reject claim 1. It is therefore submitted that the rejection of claim 1 over the combination of Walklin and Nagata should be withdrawn and that claim 1 is allowable over that

combination. The Applicant further submits that, for the same reasons that claim 1 is allowable over Walklin and Nagata, claim 17 is also allowable over Walklin and Nagata. Since claims 3-16, 19-23, and 26-31 depend variously from claims 1 and 17, it is submitted that those claims are also allowable over Walklin and Nagata.

In view of the above arguments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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